Iter.	Instruction	P (start-stop)	I (start-stop)	M (clock)	CDB-write (C)(clock)	Commit (clock)	Comments
1	L.D F2,0(R1)	1-4	2	3	4	5	
1	MUL.D F4,F2,F0						
1	L.D F6,400(R1)						
1	DIV.D F6,F4,F6						
1	S.D F6,400(R1)						
1	ADDI R1,R1,8						
1	SGTI R3,R1,800						
1	BEQ R3,R0,etic						
2	L.D F2,0(R1)						
2	MUL.D F4,F2,F0						
2	L.D F6,400(R1)						
2	DIV.D F6,F4,F6						
2	S.D F6,400(R1)						
2	ADDI R1,R1,8						
2	SGTI R3,R1,800						
2	BEQ R3,R0,etic						
3	L.D F2,0(R1)						
3	MUL.D F4,F2,F0						
3	L.D F6,400(R1)						
3	DIV.D F6,F4,F6						
3	S.D F6,400(R1)						
3	ADDI R1,R1,8						
3	SGTI R3,R1,800						
3	BEQ R3,R0,etic						

Exercize (working hypothesis)

- the pipeline implements a single-dispatch policy
- the instructions after a branch are executed speculatively
- the issue stage (I) calculates the address of the actual reads and writes;
- reads require 1 clock cycle; writes require 0 clock cycles (write buffer + split-cache);
- there's only one CDB
- dispatch stage (P) and complete stage (C) require 1 clock cycle
- there are separated integer units for the calculation of the actual address, for arithmetic and logical operations, for the evaluation of the branch condition
- the functional units do not take advantage of pipelining techniques internally (reservation stations are busy until the end of CDB-write)
- the load buffer has 5 slots
- the store buffer has 5 slots (writes wait for the operand in the store buffer, i.e., in the issue stage)
- the rest of the processor and has the following characteristics:

Type of Func.Unit	No. of Func.Units	Cycles for stage I	No. of reserv. stations
Integer (effective addr.)	1	1	2
Integer (op. A-L)	1	1	2
Integer (branch calc.)	1	1	2
FP Adder	1	4	3
FP Multiplier	1	8	3
FP Divider	1	15	2