HIGH PERFORMANCE COMPUTER ARCHITECTURE final exam 23-12-2020 **MATR.NO.**_____

SURNAME_____

FIRST NAME_____

1) (POINTS 25/40) 1) Let's consider a shared-bus shared-memory coherence protocol with the following characteristics:

- Processor Operations: Read (**PrRd**) and Write (**PrWr**).
- Bus Transactions: Read a data-block from Memory (**BusRd**), Propagate a PrWr on the bus (**BusUpd** – a single data-word goes to other caches and to memory), Write back a block onto the bus (**Flush** – the data block goes to memory).
- There are 4 states: 1) the copy is not valid (**I** – Invalid); 2) the copy is in one cache only and we assume that it has been modified even if it has been just loaded (**D** – Dirty); 3) the copy has been just loaded in the current cache and other copies exist in other caches (**S0** – shared and no other processor has updated it after loading the copy); 4) the copy is shared but some other processor had issued a write into that block (**S1** – shared and other processors issued exactly one update to that block).
- The bus has a shared line, which is activated by remote snoopers in response to a bus transaction to indicate whether (S) or not (S') other copies of the addressed block exist in other caches.

Assume that this protocol is used in a four-processor system, where each processor executes a TAS instruction to lock and gain access to an empty critical section. The initial condition is such that processor 1 has the lock and processor 2, 3, and 4 are spinning on their caches waiting for the lock to be released. Every processor gets the lock once and exits the program. These are the implementations of the lock and unlock:

```
Lock:   lw R1, mylock      # R1 = &mylock
                           bne R1, R0, Lock   # if (R1 != 0) jump to Lock
                           TAS R1, mylock     # atomically_do {R1 = &mylock; mylock = 1;}
                           bne R1, R0, Lock   # if (R1 != 0) jump to Lock
                           ret

                Unlock:    sw 0, mylock       # write 0 into &mylock
                           ret
```

Note1: the semantic of the TAS (Test And Set) instruction is the following: atomically reads the specified memory location (mylock) and writes a one into that memory location (mylock). Note2: this implementation of the Lock tries to minimize the probability to have the bus locked by the TAS (this implementation is also known as Test-and-Test-and-Set). Note3: the lock is closed when mylock==1 and it is open when mylock==0. Also assume that NO write is propagated on the bus if the TAS finds a closed lock (i.e., if the TAS fails).

By using the following tables, show the operations and bus transactions (or comments) in the best case (least number of transactions) and in the worst case (highest number of transactions)

Case A:

Bus Trans. Number	Processor Operation	P1	P2	P3	P4	Bus Transactions/Comments
---	(Init.state)	S0	S0	S0	S0	Initially, P1 holds the lock
1	sw1	S0	S1	S1	S1	**BusUpd** – P1 releases the lock

Case B:

Bus Trans. Number	Processor Operation	P1	P2	P3	P4	Bus Transactions/Comments
---	(Init.state)	S0	S0	S0	S0	Initially, P1 holds the lock
1	sw1	S0	S1	S1	S1	**BusUpd** – P1 releases the lock

2) (POINTS 15/40) Write an MPI function that reads a color array (int color[1024]) and writes an array "int histogram[256]" that contains the frequency of each of 256 possible colors (the 256 values are the value that each element of color[] can assume). A serial or serialized version **has to be avoided**. The program should be written in a way that it exploits parallelism as offered by MPI. Reference scalar version:

```
unsigned char Color[1024]; int Histogram[256];
void histo_scalar(int *histogram, unsigned char *color, int size, int wid, int nw) {
    for(int i=0; i<size; i++ ) histogram[ color[i] ]  += 1;
}
```

Hints: use send and receive to distribute the work among the available workers/nodes; use MPI primitives: **`MPI_Send, MPI_Recv, MPI_Iprobe`**.